IN THE CLAIMS

1. A method for determining data bit transition times for an incoming signal having data bits modulated by a known repeating code having a known code time period, said data bits having a known data bit time period, comprising:

integrating said incoming signal using first through Nth assumed said data bit transition times for providing first through Nth integrations, respectively; and

determining actual said data bit transition times from a certain one of said first through Nth assumed data bit transition times corresponding to a largest one of said first through Nth integrations.

2. The method of claim 1, wherein:

said N is about equal to said data bit time period divided by said code time period.

3. The method of claim 1, wherein:

integrating comprises accumulating for one or more accumulation time periods, each of said accumulation time periods about equal to said data bit time period.

4. The method of claim 1, wherein:

integrating comprises accumulating during accumulation time periods having staggered first through Nth start times for providing said first through Nth integrations, respectively, an Mth one of said start times later than an (M - 1)th one of said start times by said data bit time period divided by said N; and

determining said actual data bit transition times comprises determining said actual data bit transition times from a certain one of said first through Nth start times resulting in said largest one of said first through Nth integrations.

5. The method of claim 1, wherein:

integrating comprises generating staggered first through Nth invert times, an Mth one of said invert times later than an (M - 1)th one of said invert times by said data bit time period divided by said N; and accumulating one of (i) positive and (ii) negative accumulations before said first through Nth invert times and the other of (i) positive and (ii) negative accumulations after said first through Nth invert times for one or more accumulation time periods for providing said first through Nth integrations, respectively; and

determining said actual data bit transition times comprises determining said actual data bit transition times from a certain one of said first through Nth invert times resulting in said largest one of said first through Nth integrations.

6. The method of claim 1, wherein:

integrating comprises repetitively determining first through Nth unsigned accumulation values for said first through Nth assumed data bit transition times, respectively, for a certain number of repetitive accumulation time periods for determining first through Nth multibit unsigned accumulation values, respectively; and determining said first through Nth integrations from said

first through Nth multibit unsigned accumulation values, respectively.

7. The method of claim 1, wherein:

said actual data bit transition times are used for determining said data bits.

8. The method of claim 1, wherein:

said actual data bit transition times are used for tracking said incoming signal.

9. The method of claim 1, wherein:

said N is in a range between two and said data bit time period divided by said code time period, inclusively.

10. A method for determining data bit transition times for an incoming signal having data bits modulated by a known repeating code having a known code time period, said data bits having a known data bit time period, comprising:

integrating said incoming signal using first through Nth assumed said data bit transition times for determining one or more first through Nth unsigned accumulation values, respectively, for one or more accumulation time periods, respectively;

determining a one of said first through Nth assumed data bit transition times resulting in a largest number of largest said unsigned accumulation values; and

determining actual said data bit transition times from said one of said first through Nth assumed data bit transition times resulting in said largest number.

11. An apparatus for determining data bit transition times for an incoming signal having data bits modulated by a known repeating code having a known code time period, said data bits having a known data bit time period, comprising:

a correlation machine for integrating said incoming signal using first through Nth assumed said data bit transition times for providing first through Nth integrations, respectively; and

a data bit transition detector for determining actual said data bit transition times from a certain one of said first through Nth assumed data bit transition times corresponding to a largest one of said first through Nth integrations.

12. The apparatus of claim 11, wherein:

said N is about equal to said data bit time period divided by said code time period.

13. The apparatus of claim 11, wherein:

the correlation machine accumulates said first through Nth integrations for one or more accumulation time periods, each of said accumulation time periods about equal to said data bit time period.

14. The apparatus of claim 11, wherein:

the correlation machine integrates during accumulation time periods having staggered first through Nth start times for providing said first through Nth integrations, respectively, an Mth one of said start times later than an (M - 1)th one of said start times by said data bit time period divided by said N; and

the data bit transition detector determines said actual data bit transition times from a certain one of said first through Nth start times resulting in said largest one of said first through Nth integrations.

15. The apparatus of claim 11, wherein:

the correlation machine includes a sign inverter for generating staggered first through Nth invert times, an Mth one of said invert times later than an (M - 1)th one of said invert times by said data bit time period divided by said N; and an accumulator for accumulating one of (i) positive and (ii) negative accumulations before said first through Nth invert times and the other of (i) positive and (ii) negative accumulations after said first through Nth invert times for one or more accumulation time periods for providing said first through Nth integrations, respectively; and

the data bit transition detector determines said actual data bit transition times from a certain one of said first through Nth invert times corresponding to said largest one of said first through Nth integrations.

16. The apparatus of claim 11, wherein:

the correlation machine includes a data bit accumulator for repetitively determining first through Nth unsigned accumulation values for said first through Nth assumed data bit transition times, respectively, for repetitive accumulation time periods; and a multibit accumulator for accumulating said first through Nth unsigned accumulation values for a certain number of said accumulation time periods for determining first through Nth multibit unsigned accumulation values, respectively; and

the data bit transition detector determines said largest one of the integrations from a largest one of said first through Nth multibit unsigned accumulation values.

17. The apparatus of claim 11, further comprising:

a navigation processor for using said actual data bit transition times for determining said data bits.

18. The apparatus of claim 11, further comprising:

a navigation processor for using said actual data bit transition times for tracking said incoming signal.

19. The apparatus of claim 11, wherein:

said N is in a range between two and said data bit time period divided by said code time period, inclusively.

20. An apparatus for determining data bit transition times for an incoming signal having data bits modulated by a known repeating code having a known code time period, said data bits having a known data bit time period, comprising:

a correlation machine for integrating said incoming signal using first through Nth assumed said data bit transition times for determining one or more first through Nth unsigned accumulation values, respectively, for one or more accumulation time periods, respectively; and determining a one of said first through Nth assumed data bit transition times resulting in a largest number of largest said unsigned accumulation values; and

a data bit transition detector for determining actual said data bit transition times from said one of said first through Nth assumed data bit transition times resulting in said largest number.